What is Claimed is:

1. An output buffer with low-voltage devices to driver high-voltage signals, comprising:

a tri-state control circuit, capable of receiving and processing external low-voltage signals and high-voltage signals and outputting at least two resulting signals;

a level converter, connected to the tri-state control circuit by one end thereof, for receiving the resulting signals so as to convert low-voltage swing to high-voltage swing;

an output end module, consisting of a plurality of serial-connected metal-oxide semiconductor field effect transistors;

a first taper buffer, having one end connecting to the level converter and another end thereof connecting to the output end module; and

a second taper buffer, having one end connecting to the tri-state control circuit and another end thereof connecting to the output end module.

2. The output buffer with low-voltage devices of claim 1, wherein the maximum voltage receivable by the plural MOSFETs is 2.5V.

3. The output buffer with low-voltage devices of claim 1, wherein the output buffer is capable of driving high-voltage signals for PCI-X applications.

4. The output buffer with low-voltage devices of claim 3, wherein the output buffer is operating between 133 MHz and 66 MHz in PCI-X environment.

5. The output buffer with low-voltage devices of claim 1, wherein the output buffer is designed in a 0.13 μ m 1V/2.5V CMOS process.

6. The output buffer with low-voltage devices of claim 1, wherein the tri-state output buffer consists of a CMOS NAND gate and a CMOS NOR gate

7. The output buffer with low-voltage devices of claim 1, wherein the PMOS and NMOS transistors of the first taper buffer are 2.5V nominal Vt transistor.

8. The output buffer with low-voltage devices of claim 1, wherein the PMOS and NMOS transistors of the second taper buffer are 1V nominal Vt transistors.

9. The output buffer with low-voltage devices of claim 1, wherein the plural MOSFETs includes at least a native Vt NMOS transistor.

10. The output buffer with low-voltage devices of claim 1, wherein further includes at least a 1V NMOS transistor.

11. The output buffer with low-voltage devices of claim 1, wherein the swing voltage of the first taper buffer is 1V~3.3V.

12. The output buffer with low-voltage devices of claim 1, wherein the swing voltage of the second taper buffer is 0V~1V